

Circuit element with timing control

1. Field of the Invention

The present invention relates to a circuit element with timing control and in particular to such a circuit element which receives an external clock with a clock frequency and an associated clock period duration. The present invention can be used to advantage particularly in the area of memory elements, e.g. DRAM elements (DRAM = dynamic random access memory).

2. Background of the invention and prior art

Present day DRAM memory elements contain a plurality of chip-internal timers, i.e. on-chip timers, which control different processes running on the DRAM element. Each of these timers is subject to inaccuracies, chip area consumption and the need for standby power. Since present day DRAM memory elements are specified to operate in a wide frequency range, e.g. from 83 MHz to 167 MHz, the clock supplied to the memory element from the outside cannot be used as a time basis for the control of internal processes. In particular the external clock cannot be used to ascertain particular time periods which must be controlled on the DRAM element itself, e.g. the time t_{RAS} , which represents the time between the moment when a row (word line) is activated and the moment when this row can be precharged (closed). Another example is the time between the moment when data are written to an open row and the moment when this row should be closed; the time here is termed t_{WR} .

Traditional DRAM elements normally contain chip-internal analog timer circuits to create the necessary delays, e.g. t_{RAS} or t_{WR} . As has been explained above, these timers must

not use the externally provided clock as a time basis since the DRAM elements should be useable at different clock frequencies.

Alternative approaches have proved to be unsuitable. Such approaches include e.g. the addition of a bit line supervisor to monitor the reset voltages, but the required chip area is too large. On the other hand, the addition of a dummy bit line as reference leads to a high power consumption. Furthermore, the generation of a delay which exactly fulfils a necessary specification is too difficult to implement.

Registers have also been proposed which enable the memory control to report precisely the number of clock cycles which satisfy e.g. tRAS or TWR at the current operating frequency. This approach requires a register per timer and is therefore of no use for controlling all the timers. Also, with this approach, all the timers must be specified externally, which is not possible since not all the memory elements which satisfy a standard necessarily have the same timer structure.

As a result, today's DRAM memory elements or memory chips use independent analog delay elements to realize the above delay times, e.g. tRAS and tWR.

Summary of the invention

It is the object of the present invention to provide a device for the temporal control of at least one signal in a circuit element, which enables a compromise to be made between power consumption and accuracy.

The present invention provides a circuit element comprising:

an input for receiving an external clock with a clock period duration;

a unit for providing the circuit element with information representing the clock period duration of the external clock; and

a unit for the temporal control of at least one signal in the circuit element based on the information representing the clock period duration.

The present invention utilizes the knowledge of the clock period or the frequency of a clock signal applied externally to a circuit element in order to control exactly on this basis at least one signal in the circuit element. To this end the data indicating the clock period duration of an external clock signal are preferably stored in a memory on the circuit element, for preference a register. Preferably the circuit element also has nominal time information stored or hard-wired on it representing e.g. the specification of a predetermined delay. A timing element then uses the stored clock frequency information and the nominal time information to determine by how many clock cycles or fractions of clock cycles of the external clock signal the signal to be controlled should be delayed to achieve a specification specified by the nominal time information and to adjust the delay of a delay element in accordance with the determined clock cycles or fractions of clock cycles.

Based on the clock frequency information available according to the present invention to the circuit element, the externally provided clock signal and nominal time information optionally available on the circuit element, according to the present invention all the signals employed on the circuit element can be temporally controlled. Apart from the

specification of delay times mentioned above, this control can also include the control of the instants at which control signals in general are evoked, the duration of the same and suchlike.

In preferred embodiments the circuit element according to the present invention constitutes a memory element, e.g. a DRAM element. In preferred embodiments the DRAM element includes a register into which a value is written which represents the clock frequency and thus the clock period of an external clock signal which is supplied to the memory element. This value can be written into the register using either a chip-external or a chip-internal control. Once the value has been stored, the memory element can calculate the respective number of clock cycles needed to obtain the time instants, the time durations or the delay times which are required for internal operations and which fulfil specifications. In addition the knowledge of the clock frequency and thus of the clock period can be used to calibrate a delay component of the memory element. e.g. of the DRAM element. To reduce inaccuracies due to rounding, the memory element can employ a delay-locked loop or a phase-locked loop so as to subdivide the clock period into smaller time intervals.

Further developments of the present invention are presented in the dependent claims.

Brief Description of the Drawings:

Preferred embodiments of the present inventions are described in more detail below making reference to the enclosed drawings, in which

Fig. 1 shows a schematic representation of an embodiment of a circuit element according to the present invention;

Fig. 2 shows a table for better understanding of the present invention;

Fig. 3 shows a schematic representation of a phase-locked loop capable of being used according to the present invention; and

Fig. 4 shows a schematic representation of a delay-locked loop capable of being used according to the present invention.

Detailed Description of Preferred Embodiments

Fig. 1 shows a memory element 10, e.g.: a DRAM element. The memory element 10 might also take the more specialized form of a DDR-SDRAM element (DDR SDRAM = double data rate synchronous dynamic random access memory).

The memory element 10 receives a clock signal 12 from a clock generator 14. The clock signal represents an external clock signal and possesses a certain clock frequency. Typical clock frequencies lie in a range between 83 MHz and 167 MHz. The clock generator 14 also supplies the clock signal 12 to an external control 16. The control 16 is connected to the memory element 10 via a signal bus 18, which is usually called the CMD bus. The memory element 10 can be a memory module with a plurality of memory chips on it or a single memory chip.

The control 16 communicates with the memory element 10 via the signal bus 18 so as to transfer control signals and data signals to the memory element 10 and to receive them from it.

So far the structure of the memory element 10, clock generator 14 and control 16 described above corresponds to a traditional structure.

However, the memory element according to the present invention differs from traditional memory elements in respect of a timing control 20 for the temporal control of signals in the memory element, in the example shown so as to delay an activation signal ACT in order to generate from it the internal precharging signal PRE. The activation signal ACT is supplied to the memory element externally, usually from the memory control 16 over the CMD bus 18.

The timing control 20 includes a memory area or a register 22 in which the period duration t_{CK} of the external clock 12 is stored. In addition a memory area 24 is provided in which a nominal delay time t_{RAS} is stored which shows by how much the activation signal ACT must be delayed before it may be issued or let through as the precharging signal PRE so as to comply with the specification of the memory element 10.

The timing control 20 also includes a timing element 26, which combines the stored period duration t_{CK} and the nominal delay time so as to ascertain by how many clock cycles or fractions of clock cycles of the external clock signal 12 the activation signal ACT must be delayed to achieve a delay time which is at least equal to t_{RAS} . For this purpose the timing element includes in the simplest case a suitable combination circuit, which combines the period duration t_{CK} and the nominal delay time t_{RAS} so as to ascertain how many clock cycles of the external clock signal are necessary to realize the nominal delay time, and a delay element or a digital timer controlled by the combination circuit to delay the activation signal by the corresponding number of clock cycles of the external clock signal which is supplied to the delay element and to issue

this signal, or let it pass, as the precharging signal PRE subsequent to this delay.

Data representing the period duration of the external clock signal 12 are communicated to the memory element 10 by the memory control and stored in the clock period duration register 22 before any actual memory operations are performed. An example of how these data might be structured will now be explained in some detail making reference to Fig. 2.

In operation the memory element 10 therefore knows the clock period of the external clock signal 12 from the data stored in register 22 so that the timing element 26 can be realized using simple combinatorial logic. From the data stored in the period duration register 22 and the time information for tRAS known from the memory unit 24, the number of clock periods needed for tRAS is ascertained in order to control a delay element so that only after waiting for the ascertained number of clock periods is the activation signal ACT let through as the precharging signal PRE. The timing element 26 thus controls the output of the signal PRE on the basis of the information representing the clock period and stored in the period duration register 22.

In connection with ascertaining the number of clock periods for tRAS, the table shown in Fig. 2 should be referred to. The first column of the table represents the clock frequency fCK of the clock signal 12, where $fCK = 1/tCK$, and the second column of the table represents a multiplication factor by which the clock frequency of 118.00 MHz must be multiplied to give the clock frequency fCK in the respective line.

The third column of the table contains the data MRS stored in the clock period duration register 22. In the present case a five-bit register is used, so MRS can adopt thirty two

different values. A value 0 (not shown in the table) might e.g. indicate that no valid clock frequency information or clock period duration information has been received from the control. A value of 1 represents an external clock frequency f_{CK} between 118 MHz and 123.90 MHz, while a value of 20 stands for a clock frequency f_{CK} between 298.18 MHz and 313.09 MHz. In this way the frequency range from 118 MHz to 509.99 MHz is quantized into thirty one intervals, the size of the intervals increasing with increasing frequency.

The fourth column of the table in Fig. 2 shows the associated period duration t_{CK} in ns. In the subsequent fifth column it can be seen how many clock periods are necessary to realize a delay time t_{RAS} of 34 ns. The next two columns indicate for each interval the minimal and maximal actual time for t_{RAS} resulting from the number of period durations used. For example, in the interval from 118.00 MHz to 123.90 MHz the minimal actual time for t_{RAS} is 40.4 ns and the maximal actual time is 42.4 ns. The next, eighth column shows the maximal error in ns which results from the difference between the actual maximal time t_{RAS} and the minimal ideal value, 34 ns in the present case.

Examples of frequencies employed in actual memory implementations are shown in the column Fexamp, and the customary designations of these are given in the next column with the heading Name. Finally, the last two columns of the table give the period durations Texamp and the nominal time t_{RAS} obtained according to the present invention for the six examples.

The accuracy of the actual value of t_{RAS} derived according to the present invention depends in part on the number of bits of the clock period duration register and in part on the size of the clock period itself. The greater the number of bits of the

clock period duration register, the smaller can be the respective frequency intervals to each of which an entry is assigned in the register, so that the error of the actual value of t_{RAS} in relation to the minimal optimal value of the same decreases accordingly. The accuracy of the method used according to the present invention increases with increasing magnitude of the clock period since the rounding error is thereby reduced, as can be seen clearly from the error values shown in the eighth column of the table in Fig. 2.

The respective actual value of t_{RAS} depends on the characteristic of the memory element. The actually realized values of t_{RAS} shown in Fig. 2 are obtained in the case where only whole clock periods are used.

The accuracy can be improved by adding further bits to the clock period duration register 22.

Alternatively, the accuracy can be improved by equipping the timing element 26, which according to the present invention is preferably digitally implemented, with a time subdivision unit.

For example, a time subdivision can be achieved by means of a phase-locked loop (PLL) through which the external clock 12 is reproduced many times, thus generating a finer time basis. Thus a PLL 30 can generate a faster clock 32 from the external clock 12, as shown in Fig. 3, to generate a clock with a divided clock period. The timing element 26 then delays not by whole multiples of the external clock period but by whole multiples of the divided external clock period. The clock frequency of the fast clock 32 might e.g. be eight times the clock frequency of the external clock frequency 12, so that through this internal generation of a multiple of the external

clock frequency the accuracy of the timing control 20 can be improved considerably, so that the error which occurs is reduced accordingly.

A similar result can be achieved if a delay-locked loop (DLL) consisting of a plurality of standard delay elements or reference delay elements is provided. With the aid of the DLL the scattered delay of a standard delay element 40 (Fig. 4) due to production and operating parameters can be compared with the clock period of the external clock signal. If the delay element of the timing element 26 is now constructed from copies of these standard delay elements, the timing element can ascertain the number of standard elements 40 which must be activated in order to achieve the delay needed to satisfy the nominal time specification.

The comparison of a series of reference delays with the clock period performed in such a DLL results in a very precise step value for the timing control 20 when the clock period is known. When the actual timing control has the same delay elements, the number of elements necessary for a given operation, e.g. a given delay time t_{RAS} , can be calculated simply. In this way the rounding errors can be reduced to a fraction of a ns.

Within the framework of the description above the use of the present invention to ascertain the time t_{RAS} has been described, t_{RAS} being the time from the moment of activation of a row to the moment when this row can be precharged. If a fast autoprecharge or RAS lockout feature is activated, a Read-AP instruction can be imparted to the memory element before the time t_{RAS} has elapsed. In this case it is the task of the memory element to find the right time to automatically precharge the row. This time must be within the specification and must also enable the row information to be restored

completely. According to the present invention this right time can be ascertained by the timing element 26 according to the specification of the memory element (stored in the nominal value memory 24) and the knowledge of the external clock frequency (stored in the clock period duration register 22).

Summarizing, in the implementation described above, the control 16 determines the number (1 to 31 in the table of Fig. 2) which represents the clock period (and thus the clock frequency) of the clock signal 12 with which the memory element is actually operated. This number is communicated to the DRAM memory element 10 over the command bus and is there stored, as has been described above, in the period duration register, which may be a field of a mode register. The memory element then ascertains, from the number stored in the mode register and respective internal times, e.g. t_{RAS} , a number of clock periods or partial clock periods ascertained from the clock periods if a DLL or a PLL is employed, in order to control on this basis a preferably digital delay element.

The principle described above in respect of the time t_{RAS} can be used to control signals of all kinds in the circuit element or memory element.

For example, the principle can be used to ascertain t_{WR} , i.e. the time which must elapse before a row can be closed after a write operation. Normally a read or write instruction with "autoprecharge" is received by a DRAM element and the element performs an internal precharge at time t_{WR} after the read/write instruction. This time t_{WR} can again, according to the explanation above, be ascertained by ascertaining an assigned number of clock periods, the period duration stored in the clock frequency register 22 being known.

Furthermore, the present invention can be used advantageously in the case of self refresh. For example, a DRAM must execute an autorefresh instruction within predetermined intervals in order to perform a self refresh. In normal operation the memory control or the memory controller must present this autorefresh instruction to the memory externally. A typical interval for performing such a refresh is 7.8 μ s. In the self refresh mode the DRAM memory must generate an internal autorefresh instruction internally every 7.8 μ s. The self refresh mode is activated after an SRF instruction has been received from the control, after which the external clock can be disconnected. Until now a corresponding autorefresh instruction was generated every 7.8 μ s with the aid of an analog timer. According to the present invention the memory element calibrates an analog timer with the knowledge of the clock period stored in the clock period duration register. Thus the respective time for the autorefresh instruction, i.e. $t_{REFRESH}$, can be ascertained more exactly. The invention can also be used to control the instants for a staggered refresh of a plurality of independent memory banks with a single autorefresh command. This enables refresh current peaks to be reduced and the internal voltage generator system can be made smaller, thus economizing on rest current and chip area.

In addition to the above examples t_{RAS} , t_{WR} , $t_{REFRESH}$ and t_{RFC} the present invention can be used to control internal signals of all kinds in a circuit element and in particular in a memory element.

Apart from the register for storing the clock frequency information or clock period information described above, the corresponding information can also be made available on the circuit element in other ways. For example, it is possible to program the desired time (e.g. t_{RAS}) with laser fuses or some other non-volatile storage method during the manufacturing

process. In a final process step during manufacture memory elements which have hitherto been manufactured identically can be adjusted for different speed classes.

Additionally, it is possible to provide a further register into which the memory control writes the speed class information. With only a few registers it is then possible for many or all timers, i.e. timing elements, of a memory element to be retarded or accelerated in that delay elements of the same are controlled in the light of the chosen speed class information and the external clock which is actually used.

In already existing memory modules (DIMMs) there is an EEPROM in which various time constants which are characteristic for a DRAM and which are guaranteed by the manufacturer are stored. This EEPROM is inscribed by the manufacturer after the final test. In present systems, however, the memory chip or memory element has no knowledge of the content of this EEPROM. The register referred to above offers the memory control the possibility of communicating the values read out of the EEPROM, e.g. the speed class, to the memory chip since they can be written into this register. The memory chip can then adjust the internal timing elements or timers adequately using this information.